ABSTRACT OF THE DISCLOSURE

A memory cell array has a unit formed from one memory cell and two select transistors sandwiching the memory cell. One block has one control gate line. Memory cells connected to one control gate line form one page. A sense amplifier having a latch function is connected to a bit line. In a data change operation, data of memory cells of one page are read to the sense amplifiers. After data are superscribed on data in the sense amplifiers, and a page erase is performed, data in the sense amplifiers are programmed in the memory cells of one page. Superscription of data in the sense amplifiers allows a data change operation for byte data or page data.